IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Applicant:	Paul A. LaBerge	§	Art Unit:	2833
Serial No.:	09/363,605	§	Examiner:	Xuong M. Chung-Trans
Filed:	July 29, 1999	§		
Title:	Capturing Read Data	§	Docket No.	MCT.0078US (70-0130.00/US)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

DRAFT

PROPOSED AMENDMENT

Dear Sir:

The following proposed amendment is in response to a telephone conversation between the undersigned and Examiner Lefkowitz on January 15, 2004. Based on this conversation, the following CLAIM AMENDMENTS section contains suggested amendments to the claims. The comments in the REMARKS section explain the proposed amendment.

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Janice Munoz

CLAIM AMENDMENTS

1. (Currently Amended) A computer system comprising:

a local bus;

a memory bus capable of indicating data; ~~and~~

a first buffer adapted to capture the data directly from the memory bus, the buffer being located closer to the local bus than to the memory bus; and

a memory interface located closer to the memory bus than to the local bus, the memory interface including a second buffer to store other data to be furnished to the memory bus.

2. (Currently Amended) The computer system of claim 1, wherein

the memory bus is capable of indicating a data strobe signal, and

the first buffer is adapted to latch the data from the memory bus in response to the data strobe signal.

3. (Currently Amended) The computer system of claim 1, further comprising:

conductive traces adapted to communicate indications of the data from a first region located closer to the memory bus than to the first buffer to a second region located closer to the first buffer than to the memory bus, the conductive traces introducing an approximate first asynchronous propagation delay in the communication.

4. (Currently Amended) The computer system of claim 3, further comprising:

circuitry adapted to transfer the data from the first buffer to the local bus without introducing a second propagation asynchronous propagation delay that is greater than the first asynchronous propagation delay.

5. (Currently Amended) The computer system of claim 1, wherein the first buffer is part of a local bus interface.

6. (Currently Amended) The computer system of claim 1, further comprising:

circuitry adapted to transfer the data from the first buffer to the local bus, at least a portion of the circuitry being synchronized to a clock signal and the circuitry adapted to transfer the data without introducing an asynchronous propagation delay greater than approximately one cycle of the clock signal.

7. (Currently Amended) The computer system of claim 1, wherein the first buffer is part of a local bus interface that is coupled to the local bus, the computer system further comprising:

a third bus;

a fourth bus;

a third bus interface coupled to communicate with the third bus;

a fourth bus interface coupled to communicate with the fourth bus; and

a multiplexing circuit adapted to selectively cause the first buffer to store other data from the third and fourth bus interfaces.

8. (Currently Amended) The computer system of claim 1, wherein the first buffer is part of a local bus interface that is located closer to the local bus than to the memory bus.

9. (Original) The computer system of claim 8, wherein the local bus interface further comprises:

a local bus controller adapted to use the first buffer to furnish signals to the local bus that indicate the data.

10. (Cancelled)

11. (Currently Amended) A bridge for use with a local bus and a memory bus capable of indicating data, comprising:

conductive traces adapted to communicate indications of the data from a first region closer to the memory bus than the local bus to a second region located closer to the local bus than to the memory bus; and

a local bus interface being located closer to the local bus than to the memory bus, the local bus interface including a first buffer adapted to capture the indications of the data from the conductive traces near the second region to directly capture the data from the memory bus; and

a memory interface located spatially closer to the memory bus than to the local bus, the memory interface including a second buffer to store other data to be furnished to the memory bus.

12. (Currently Amended) The bridge of claim 11, wherein

the memory bus is capable of indicating a data strobe signal, and

the first buffer is adapted to latch the data in response to the data strobe signal.

13. (Currently Amended) The bridge of claim 11, wherein the conductive traces introduce a first asynchronous propagation delay to the indications of the data, the bridge further comprising:

circuitry adapted to transfer the data from the first buffer to the local bus without introducing a second asynchronous propagation delay that is greater than the first asynchronous propagation delay.

14. (Currently Amended) The bridge of claim 13, further comprising:

circuitry adapted to transfer the data from the first buffer to the local bus, at least a portion of the circuitry being synchronized to a clock signal and the circuitry adapted to transfer the data without introducing an asynchronous propagation delay greater than approximately one cycle of the clock signal.

15. (Currently Amended) The bridge of claim 12, further comprising:

a third bus;

a fourth bus;

a third bus interface coupled to communicate with the third bus;

a fourth bus interface coupled to communicate with the fourth bus; and

a multiplexing circuit adapted to selectively cause the first buffer to store other data from the third and fourth bus interfaces.

16. (Currently Amended) The bridge of claim 12, wherein the local bus interface further comprises:

a local bus controller adapted to use the first buffer to furnish signals to the local bus that indicate the data.

17. (Cancelled)

18. (Currently Amended) A method usable with a computer system that includes a local bus and a memory bus, the method comprising:

furnishing data to the memory bus in a memory read operation; and

capturing the data directly from the memory bus in a first buffer that is located closer to the local bus than to the memory bus; and

furnishing other data to the memory bus from a second buffer that is located in a memory interface, the memory interface being located closer to the memory bus than to the local bus.

19. (Original) The method of claim 18, wherein the act of capturing comprises:

latching the data from the memory bus in response to a data strobe signal of the memory bus.

20. (Currently Amended) The method of claim 18, further comprising:

using conductive traces adapted to communicate indications of the data from a first region located closer to the memory bus than to the first buffer to a second region located closer to the first buffer than to the memory bus, the conductive lines introducing an approximate first asynchronous propagation delay in the communication.

21. (Currently Amended) The method of claim 20, further comprising:

transferring the data from the first buffer to the local bus without introducing a second asynchronous propagation delay that is greater than the first asynchronous propagation delay.

22. (Currently Amended) A method usable with a computer system, comprising:

extending a memory bus into a bridge, the memory bus being adapted to indicate data in a memory read operation; and

capturing the data directly from the extension of the memory bus into a first buffer of the bridge, the first buffer being located closer to a local bus than to the memory bus; and

furnishing other data to the memory bus from a second buffer located inside a memory interface, the memory interface being located closer to the memory bus than to the local bus.

23. (Original) The method of claim 22, wherein the act of capturing comprises:

latching the data from the extension of the memory bus in response to a data strobe signal of the memory bus.

24.-25. (Cancelled)

26. (Currently Amended) The method of claim 22, wherein the act of extending comprises:

extending the memory bus into the bridge so that the extended end of the memory bus is closer to [[a]] the local bus than to the portion of the memory bus that is located outside of the bridge.

27. (Currently Amended) The method of claim 18, further comprising:

transferring the data from the first buffer to the local bus; and

synchronizing the transferring to a clock signal,

wherein the transferring occurs without introducing an asynchronous propagation delay greater than approximately one cycle of the clock signal.

28. (Currently Amended) The method of claim 22, further comprising:

transferring the data from [[a]] the second buffer to [[a]] the local bus; and, ~~the buffer being located closer to the memory bus than to the local bus; and~~

synchronizing the transferring to a clock signal,

wherein the transferring occurs without introducing an asynchronous propagation delay greater than approximately one cycle of the clock signal.

REMARKS

In a telephone conversation between the undersigned and Examiner Lefkowitz on January 15, 2004, the Examiner stated that independent claim 1 would be allowable if the limitations of dependent claim 10 were incorporated into independent claim 1. Furthermore, Examiner Lefkowitz stated that if the limitations of claim 17 were incorporated into claim 11 (without requiring the incorporation of the limitations from dependent claim 16), independent claim 11 would be allowable. Thus, olaim 1 has been amended to incorporate the limitations of dependent claim 10, expect that the nomenclature "first buffer" and "second buffer" has been used to resolve any potential antecedent basis problems. Dependent claims from independent claims 1 and 17 have been amended to be consistent with the new language of the independent claims.

Similar limitations have been added to the method claims, independent claims 18 and 22. Claims that depend from independent claims 18 and 22 have been amended to resolve any potential indefiniteness problems associated with these claims.

Please feel free to contact the undersigned at (713) 468-8880, extension 303 to discuss the proposed amendment.

Respectfully submitted,

Date: January 16, 2004

DRAFT

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INTERVIEW SUMMARY

Dear Sir:

The conversation between Examiner Lefkowitz and the undersigned on January 15, 2004, is summarized in the following REMARKS section.

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Janice Munoz

REMARKS

In a telephone conversation between the undersigned and Examiner Lefkowitz on January 15, 2004, the Examiner stated that independent claim 1 would be allowable if the limitations of dependent claim 10 were incorporated into independent claim 1. Furthermore, Examiner Lefkowitz stated that if the limitations of claim 17 were incorporated into claim 11, (without requiring the incorporation of the limitations from dependent claim 16), independent claim 11 would be allowable.

Other than claims 1, 10, 11, 17, 18 and 22, no other claims were discussed with Examiner Lefkowitz. Examiner Lefkowitz also stated that if Applicants desire to maintain the appeal, the claims would be rejected under 35 U.S.C. § 103 in view of U.S. Patent No. 5,394,519 (Bodin) as the primary reference. No other claims or prior art were discussed between the undersigned and Examiner Lefkowitz.

Respectfully submitted,

Date: January 16, 2004

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